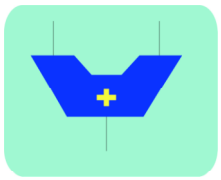

VLSI Society of India
http://vlsi-india.net/vsi

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VLSI Society of India,
IEEE Circuits and Systems Society (Bangalore Chapter),
and
IEEE Electron Devices and Solid State Circuits Society (Bangalore Chapter)

are happy to announce

A TWO-DAY WORKSHOP
ON
LOW POWER DESIGN TECHNIQUES

Venue – Golden Jubilee Hall, Indian Institute of Science, Bangalore
Date – Feb 25-26 (Friday-Saturday)
Time – 9.00 – 6.00 PM

SPEAKERS

Prof. Christian Piguet. Prof. Piguet joined the Centre Electronique Horloger S.A., Neuchâtel, Switzerland, in 1974. He worked on CMOS digital integrated circuits for the watch industry, low-power embedded microprocessors and CAD tools based on a gate matrix approach. Prof. Piguet is now Head of the Ultra-Low-Power Sector at the CSEM (Centre Suisse d'Electronique et de Microtechnique S.A), Neuchâtel, Switzerland. He is presently involved in design and management of low power and high speed integrated circuits in CMOS technology. His main interests include design of very low-power microprocessors, low-power standard cell libraries, gated clock and low-power techniques as well as asynchronous design. He is Professor at the Ecole Polytechnique Fédérale Lausanne (EPFL), Switzerland, he also lectures in VLSI and microprocessor design at the University of Neuchâtel, Switzerland, as well as other postgraduate courses in low-power design.

Dr. Kiyoo ITOH has been leading RAM technology at Hitachi Ltd: He was the lead designer of the first prototype for eight generations of Hitachi DRAMs ranging from 4Kb to 64Mb. He initiated circuit inventions and developments to reduce sub-threshold current of MOSFETs even for the active mode, which is highlighted today in low-voltage CMOS LSI design. Typical examples of the reduction circuits are the dynamic substrate back-bias control, multi-threshold (Vt) CMOS logic, various gate-source (self) back-biasing schemes, and power switch that we take for granted today. He holds over 370 patents in Japan and US. He authored three books and one book chapter on memory designs, and contributed over 130 technical papers and presentations, many of them invited, in IEEE journals and conference proceedings. Dr. Itoh has won 16 honors in US, Europe, and Japan. They include the IEEE Paul Rappaport Award in1984, the Best Paper Award of ESSCIRC90, and the 1993 IEEE Solid-State Circuits Award. He is an IEEE Fellow. In Japan, his awards include the National Invention Award (Prize of the Patent Attorney's Association of Japan) in 1989, the Commendation by the Minister of State for Science and Technology (Person of Scientific and Technological Merits) in 1997, and the National Medal of Honor with Purple Ribbon in 2000.

V. Ramgopal Rao is an Associate Professor in the Department of Electrical Engineering, IIT Bombay. He has over 140 publications in these areas in refereed international journals and conference proceedings and holds two patents. Prof. Rao is an Editor for the IEEE Transactions on Electron Devices in the CMOS Devices and Technology area and is a Distinguished Lecturer (DL), IEEE Electron Devices Society. He is a Senior Member, IEEE and a Fellow, IETE. Dr. Rao received the Swarnajayanti Fellowship award for 2003-2004, instituted by the Department of Science and Technology, Govt. of India. He is also a working group member setup by the Govt. of India on Nanotechnology. Prof. Rao was the organizing committee chair for the 17th International Conference on VLSI Design, and was Chairman, IEEE AP/ED Bombay Chapter during 2002-2003.

Dr. V. Visvanathan is a Distinguished Member of Technical Services at Texas Instruments India, where he serves as the Chief Technologist in ASIC Product Development Center. He works on CAD flow-related issues for comprehending deep submicron problems into the SoC Design Flow. At TI, he has worked on problems related to signal integrity, design closure, dynamic IR drop, and power integrity. Before joining TI, he has served at Cadence and at AT&T Bell Labs. He was also a Professor in the CAD Center at the Indian Institute of Science.

Several speakers from VLSI industry are expected to participate. Updates will be announced on VSI Website.

Program:

Day 1 – Low-Power Analog Design

08.30 AM – 09.30 AM	*Registration*
09.30 AM – 11.00 AM	*Session I – Introduction to Low-Power Design*
11.00 AM – 11.30 AM	*Tea Break and Time for Interaction*
11.30 AM – 1.00 PM	*Session II – Ensuring Power Integrity: Analysis and Closure Challenges*
1.00 PM – 02.00 PM	*Lunch and Time for Interaction*
02.00 PM – 04.00 PM	*Session III – Novel Device Architectures and Processes for the 65 nm CMOS Technology Node and Beyond*
04.00 PM – 04.30 PM	*Tea Break*
04.30 PM– 06.00 PM	*Session IV - Power Management in Mixed Signal Circuits*

Day 2 – Low-Power Digital Design

08.30 AM – 09.30 AM	*Registration*
09.30 AM – 11.00 AM	*Session V – Leakage Reduction in Low-Voltage Embedded RAMs*
11.00 AM – 11.30 AM	*Tea Break*
11.30 AM – 01.00 PM	*Session VI – Dynamic and Static Power Reduction Techniques*
01.00 PM – 02.00 PM	*Lunch*
02.00 PM – 03.30 PM	*Session VII – Low-Power Design Techniques*
03.30 PM – 04.00 PM	*Tea Break*
04.00 PM– 06.00 PM	*Session VIII – Open Discussion on Low-power Digital Design*

Registration Details

	Student/Faculty	**Others - VSI/IEEE Member***	**Others – Non Members***
Before Jan 31, 2005	Rs 500/-	Rs 2000/-	Rs 3000/-
After Jan 31, 2005	Rs 1000/-	Rs 3000/-	Rs 4000/-
**Single-day registration is permitted at 50% of the rate. Clearly indicate the day for which you are registering.*			

*Draft/Cheque should be made out to "**VLSI Society of India**" and must be sent to Mr Mohan Kumar, Finance, VLSI Society of India, Texas Instruments India, Bagmane Tech Park, CV Raman Nagar, Bangalore 560093. Please include the participant's name, e-mail address, contact address, phone and FAX numbers, and professional status. Write "Low Power Workshop, Feb 2005" on the top of the application form and behind the draft. Clearly indicate the name(s) of the participant(s) if you are sending bulk registrations from the same organization. The registration fee includes registration material and lunch/tea on the day(s) for which you have registered. You are responsible for making your own arrangements for stay and travel. Receipts for the payment and participation certificates will be made available at the workshops. The number of participants will be limited; send your registrations to reach before Feb 10, 2005. Confirmations will be sent by email only. Queries about the tutorial must be sent only to lpd05@hotmail.com .*

***Venue Information** – The Indian Institute of Science is located near Malleshwaram/Yeshavantpur in Bangalore. The approximate distance from the Railway station is about 5 km, and from the Airport is about 15 km. The locals refer to IISc as "Tata Institute". The weather in Bangalore during February is pleasant and nights are chilly.*